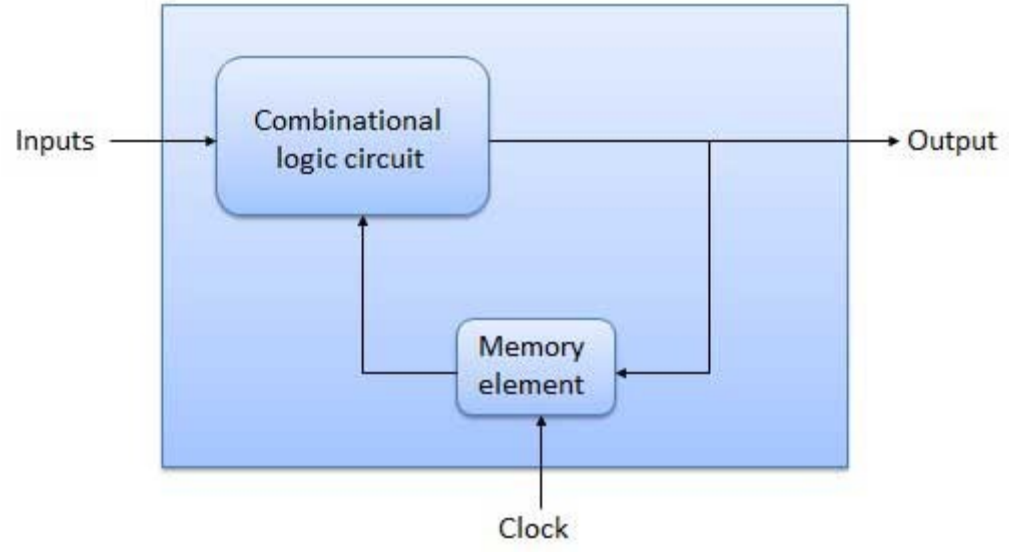
Latches and flip flops

Sequential Circuits

The combinational circuit does not use any memory. Hence the previous state of input does not have any effect on the present state of the circuit. But sequential circuit has memory so output can vary based on input This type of circuits depends upon present input as well as previous output, clock.

combinational circuit किसी भी मेमोरी का उपयोग नहीं करता है। इसलिए इनपुट की previous state का सर्किट की present state पर कोई प्रभाव नहीं पड़ता है। लेकिन sequential circuit में मेमोरी होती है इसलिए आउटपुट , इनपुट के आधार पर भिन्न हो सकते हैं। इस प्रकार के सर्किट present input के साथ-साथ पिछले previous output, clock पर भी निर्भर करते हैं।



Latches and flip-flops

In the same way that gates are the building blocks of combinatorial circuits, latches and flip-flops are the building blocks of sequential circuits.(जिस तरह से गेट्स combinatorial circuits के बिल्डिंग ब्लॉक्स हैं, उसी प्रकार latches और flip-flops sequential circuits के बिल्डिंग ब्लॉक हैं।)

Gates are built directly from transistors and latches can be built from gates, and flip-flops can be built from latches. (Gates सीधे ट्रांजिस्टर से बनाए जाते हैं और गेट से latches बनाए जा सकते हैं और latches से फ्लिप-फ्लॉप बनाए जा सकते हैं।)

Both latches and flip-flops are circuit elements whose output depends not only on the current inputs, but also on previous inputs and outputs. The difference between a latch and a flip-flop is that a latch does not have a clock signal, whereas a flip-flop has a clock signal. (लैच और फ्लिप-फ्लॉप दोनों circuit elements हैं जिनका आउटपुट न केवल current inputs पर निर्भर करता है, बल्कि previous inputs and outputs पर भी निर्भर करता है। latch and a flip-flop के बीच का अंतर यह है कि एक latch में a clock signal नहीं होता है, जबकि एक फ्लिप-फ्लॉप में एक a clock signal होता है।)

Latches are asynchronous, which means that the output changes very soon after the input changes.(Latches asynchronous हैं, जिसका अर्थ है कि इनपुट में परिवर्तन के तुरंत बाद आउटपुट में परिवर्तन होता है।)

A flip-flop is a synchronous version of the latch.(एक फ्लिप-फ्लॉप the latch का एक synchronous version है।)

A latch is a bistable multivibrator. which has two stable states namely high output as well as low-output. This includes a feedback lane by which data can be stored with the device. A latch is a memory device used to store one bit of data. These are same like flip-flops, however, they are not synchronous devices. They do not work on edges of the clock as Flip Flop do. (latch एक bistable multivibrator है। जिसमें two stable states हैं जैसे high output और साथ ही as low-output । इसमें एक feedback lane शामिल है जिसके द्वारा डिवाइस के

साथ डेटा संग्रहीत किया जा सकता है। latch एक मेमोरी डिवाइस है जिसका उपयोग एक बिट डेटा को स्टोर करने के लिए किया जाता है। ये फ्लिप-फ्लॉप के समान हैं, हालांकि, वे सिंक्रोनस डिवाइस नहीं हैं। latch edges of the clock पर काम नहीं करते हैं जैसा कि फ्लिप फ्लॉप करते हैं।)

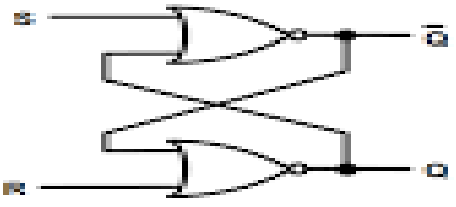


Figure 4.1 SR NOR Latch

S	R	Q	Q̄
0	0	Q	Q̄
0	1	0	1
1	0	1	0
1	1	0	0

Table 4.1 SR NOR Latch Truth Table

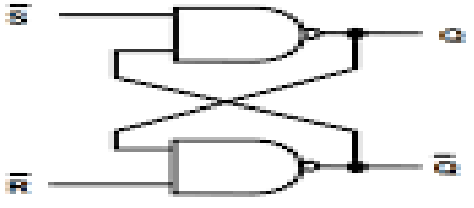


Figure 4.2 SR NAND Latch

S̄	R̄	Q	Q̄
1	1	Q	Q̄
0	1	1	0
1	0	0	1
0	0	1	1

Table 4.2 SR NAND Latch Truth Table

This latch is called *SR-latch*, which stands for *set* and *reset*.

Latches are level triggered . (Latches level triggered होते है)

Flip Flop

A Flip-Flop or FF is a couple of latches, and the designing of this can be done using a NOR gate or a NAND gate.(Flip-Flop or FF is एक of latches है, और इस का डिज़ाइन NOR गेट या NAND गेट का उपयोग करके किया जा सकता है।)

FF can have 2-inputs, 2-outputs, a set as well as reset.(FF में 2-इनपुट, तथा 2-आउटपुट होते जिससे सेट और साथ ही रीसेट हो सकते हैं।)

The main function of the flip-flop is to store the binary values (फ्लिप-फ्लॉप का मुख्य कार्य बाइनरी values को संग्रहीत करना है)

A Flip-Flop will have an extra CLK signal to make it work in a different way when contrasted with a latch. (फ्लिप-फ्लॉप में एक अतिरिक्त CLK होता है जी की latch से contrasted होने पर भी different तरह से work करता है.)

Flip flop is a sequential circuit which generally samples its inputs and changes its outputs only at particular instants of time and not continuously. Flip flop is edge sensitive or edge triggered. (फ्लिप फ्लॉप एक sequential circuit है जो आम तौर पर अपने inputs लेता है और केवल particular instants of time पर अपने आउटपुट को बदलता है और लगातार नहीं। फ्लिप फ्लॉप edge sensitive or edge triggered होते है।)

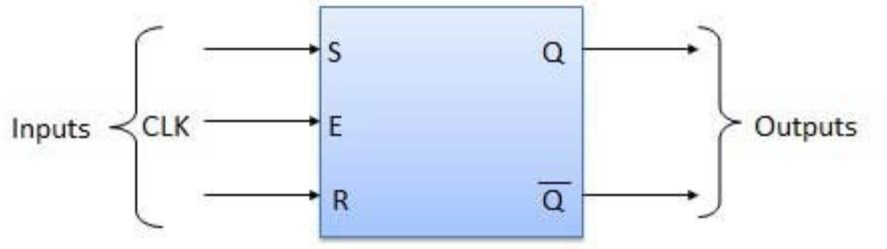
Types of flip flop :-

There are 4 types of flip flop
1- S-R FLIP FLOP
2- J-K FLIP FLOP
3- D FLIP FLOP
4- T FLIP FLOP

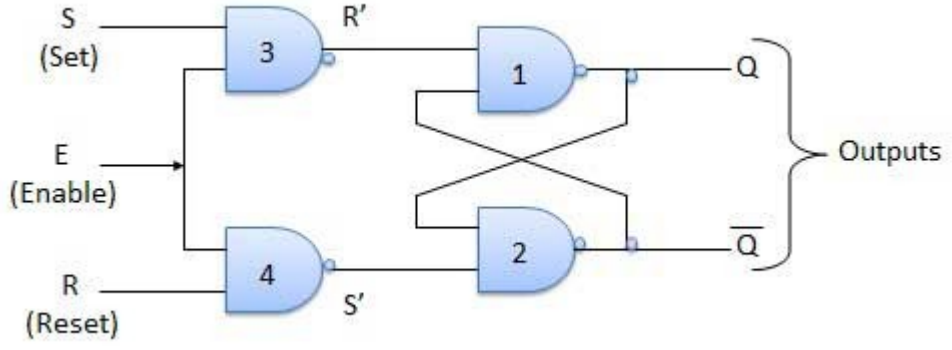
S-R Flip Flop-

It is basically S-R latch using NAND gates with an additional **enable** input. It is also called as level triggered SR-FF. For this, circuit in output will take place if and only if the enable input (E) is made active. In short this circuit will operate as an S-R latch if E = 1 but there is no change in the output if E = 0. (यह मूल रूप से एक S-R latch जिसमे additional **enable** input दिया गया है। इसे level triggered SR-FF भी कहा जाता है। इस circuit में , आउटपुट तब take place होता है जब सर्किट में केवल और केवल enable input (E) active किया जाता है। संक्षेप में, यह सर्किट तब कार्य करता है जब S-R latch E = 1 होगा लेकिन यदि E = 0 हो तो आउटपुट में कोई परिवर्तन नहीं होता है)

Block Diagram



Circuit Diagram



Truth Table

Inputs			Outputs		Comments
E	S	R	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	0	Q_n	$\overline{Q}_n$	No change
1	0	1	0	1	Rset
1	1	0	1	0	Set
1	1	1	x	x	Indeterminate

Operation

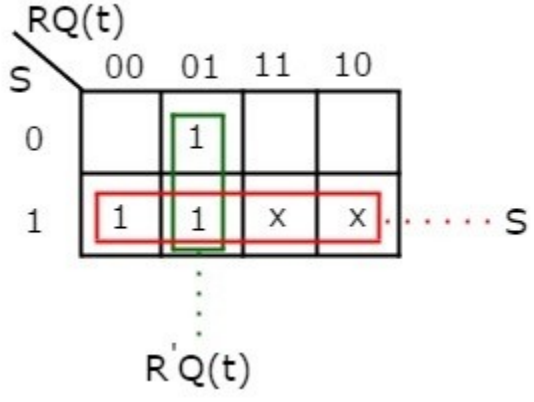
S.N.	Condition	Operation
1	**S = R = 0 : No change**	If S = R = 0 then output of NAND gates 3 and 4 are forced to become 1.Hence R' and S' both will be equal to 1. Since S' and R' are the input of the basic S-R latch using NAND gates, there will be no change in the state of outputs. (यदि S = R = 0 हो तो NAND गेट 3 और 4 का आउटपुट 1 होगा ।

		इसलिए R 'और S' दोनों 1 के बराबर होंगे। चूंकि S 'और R' NAND गेट्स का उपयोग basic S-R latch के इनपुट में होता है हैं, इसलिए आउटपुट की स्थिति में कोई बदलाव नहीं होगा।)
2	**S = 0, R = 1, E = 1**	Since S = 0, output of NAND-3 i.e. R' = 1 and E = 1 the output of NAND-4 i.e. S' = 0. Hence Q_{n+1} = 0 and Q_{n+1} bar = 1. This is reset condition. S=0 होने पर गेट 3 का output R'= 1 होगा . और E = 1 होने पर NAND-4 i.e. S' का आउटपुट 0 होगा . अत Q_{n+1} = 0 and Q_{n+1} bar = 1 होगा . This is reset condition
3	**S = 1, R = 0, E = 1**	Output of NAND-3 i.e. R' = 0 and output of NAND-4 i.e. S' = 1. Hence output of S-R NAND latch is Q_{n+1} = 1 and Q_{n+1} bar = 0. This is the set condition. S=1 होने पर गेट 3 का output R'= 0 होगा . और E = 1 होने पर NAND-4 i.e. S' का आउटपुट 1 होगा . अत Q_{n+1} = 1and Q_{n+1} bar = 0 होगा . This is set condition.
4	**S = 1, R = 1, E = 1**	As S = 1, R = 1 and E = 1, the output of NAND gates 3 and 4 both are 0 i.e. S' = R' = 0. Hence the **Race** condition will occur in the basic NAND latch S = 1, R = 1 and E = 1 होने पर of NAND gates 3 and 4 का output 0 होगा i.e. S' = R' = 0. Hence the **Race** condition will occur in the basic NAND latch.

characteristic table of SR flip-flop

Present Inputs		Present State	Next State
S	**R**	**Q**tt	**Q**t+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

By using three variable K-Map, we can get the simplified expression for next state, Qt+1t+1. The **three variable K-Map** for next state, Qt+1t+1 is shown in the following figure.



The maximum possible groupings of adjacent ones are already shown in the figure. Therefore, the **simplified expression** for next state Qt+1 is

$$Q(t+1)=S+R'Q(t)$$

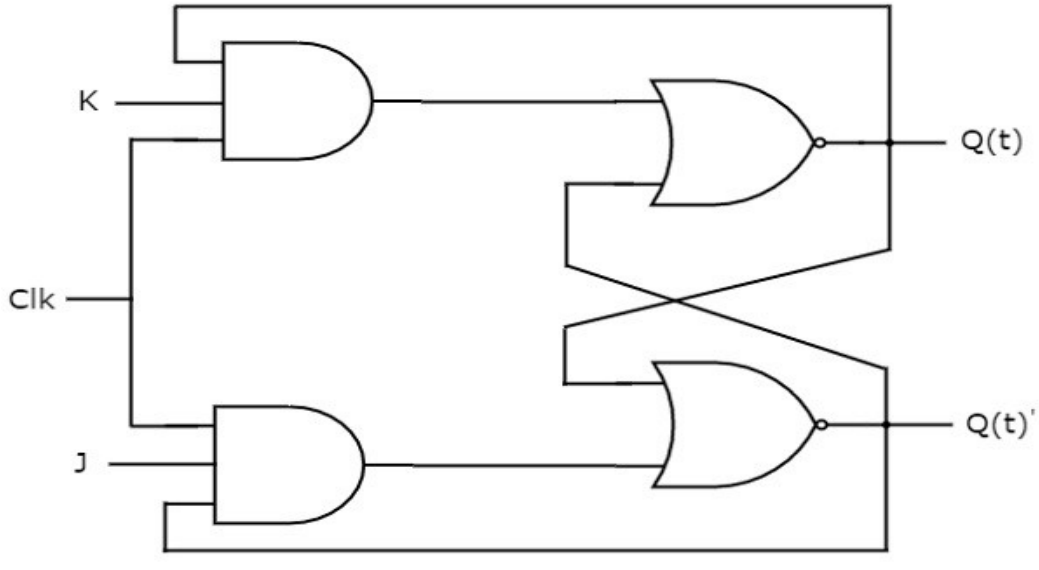
. The main problem with R-S flip flops is the indeterminate states. To avoid them, either use a clocked R-S flip flop or, better to use a J-K FLIP FLOP.(R-S flip flops के साथ मुख्य समस्या

indeterminate states की है। उनसे बचने के लिए, या तो J-K FLIP FLOP का उपयोग या clocked R-S फ्लिप फ्लॉप का उपयोग करना चाहिए)

JK Flip-Flop

JK flip-flop is the modified version of SR flip-flop. It operates with only positive clock transitions or negative clock transitions. (जेके फ्लिप-फ्लॉप

JK flip-flop of SR flip-flop का संशोधित संस्करण है। यह केवल positive clock transitions या or negative clock transitions से संचालित होता है।) The circuit diagram of JK flip-flop is shown in the following figure.



This circuit has two inputs J & K and two outputs Qt & Qt'. The operation of JK flip-flop is similar to SR flip-flop. to considered the inputs of SR flip-flop as S = J Qt' and R = KQt in order to utilize the modified SR flip-flop for 4 combinations of inputs.

इस सर्किट में दो इनपुट J & K और दो आउटपुट Qt & Qt' हैं। JK flip-flop का संचालन SR flip-flop के समान है। इनपुट के 4 संयोजनों बनाने हेतु modified SR फ्लिप-फ्लॉप का उपयोग करने के लिए SR फ्लिप-फ्लॉप के इनपुट को S = J Qt 'और R = KQt माना है ।

The following table shows the **state table** of JK flip-flop.

J	K	Qt+1

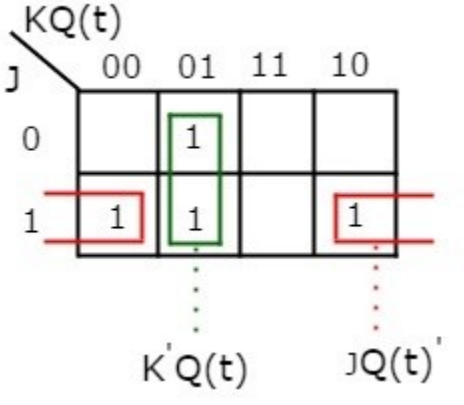
0	0	Qt
0	1	0
1	0	1
1	1	Qt'

Here, Qt & Qt+1 are present state & next state respectively. यहाँ, Qt & Qt + 1 क्रमशः present state & next state है.

The following table shows the **characteristic table** of JK flip-flop.

Present Inputs		**Present State**	**Next State**
J	**K**	**Q**tt	**Q**t+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

By using three variable K-Map, we can get the simplified expression for next state, Qt+1t+1. **Three variable K-Map** for next state, Qt+1t+1 is shown in the following figure.



The maximum possible groupings of adjacent ones are already shown in the figure. Therefore, the **simplified expression** for next state Qt+1 is

$$Q(t+1)=JQ(t)'+K'Q(t)$$

Advantages

1. Among the basic flip-flops the J-K flip-flop is the most versatile.
2. It is an improved variation of the SR Flipflop.

Disadvantages

1. An unstable state occurs when both J and K inputs are logic '0.

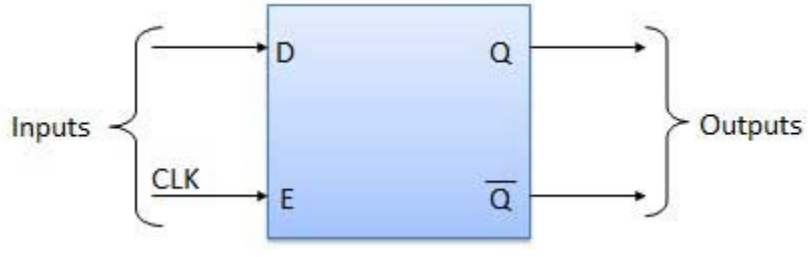
Delay Flip Flop / D Flip Flop

Delay Flip Flop or D Flip Flop is the simple gated S-R latch with a NAND inverter connected between S and R inputs. It has only one input. The input data is appearing at the output after some time. Due to this data delay between i/p and o/p, it is called delay flip flop. S and R will be the complements of each other due to NAND inverter. Hence S = R = 0 or S = R = 1, these input condition will never appear. This problem is avoid by SR = 00 and SR = 1 conditions.

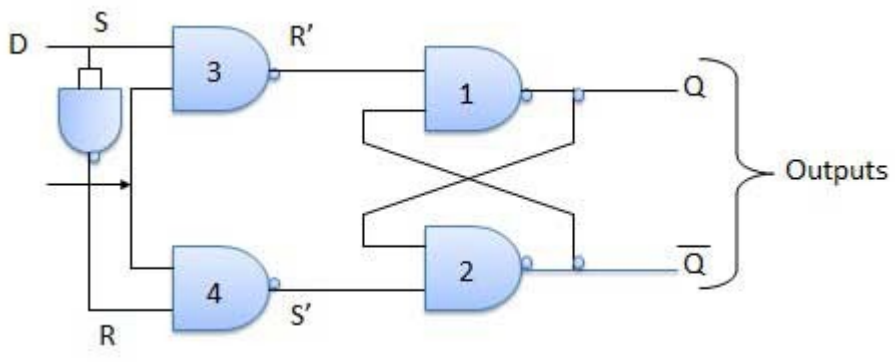
(Delay Flip Flop or D Flip Flop एक simple gated S-R latch जिसके S and R inputs में NAND inverter connect होता है । इसका केवल एक इनपुट होता है। input data कुछ समय बाद output पर दिखाई देता है। I / p और o / p के बीच इस data delay के कारण, इसे delay flip flop कहा जाता है। NAND inverter के कारण S और R एक दूसरे के complements होंते है । इसलिए S = R = 0 या S = R = 1, ये इनपुट स्थिति कभी appear नहीं होगी। यह समस्या SR = 00 और SR = 1 स्थितियों से avoid किया जाता है।)

D flip-flop operates with only positive clock transitions or negative clock transitions. D flip-flop केवल positive clock transitions negative clock transitions में काम करता है

Block Diagram



Circuit Diagram



Truth Table

Inputs		Outputs		Comments
E	D	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	0	1	Rset
1	1	1	0	Set

Operation

S.N.	Condition	Operation
1	**E = 0**	Latch is disabled. Hence no change in output . Latch is disabled है। इसलिए आउटपुट में कोई बदलाव नहीं होता है ।
2	**E = 1 and D = 0**	If E = 1 and D = 0 then S = 0 and R = 1. Hence irrespective of the present state, the next state is Q_{n+1} = 0 and Q_{n+1} bar = 1. This is the reset condition. यदि E = 1 and D = 0 then S = 0 and R = 1 है . इसलिए present state के बावजूद, next state Qn + 1 = 0 और Qn + 1 bar = 1 होता है .अत: यह रीसेट स्थिति है।
3	**E = 1 and D = 1**	If E = 1 and D = 1, then S = 1 and R = 0. This will set the latch and Q_{n+1} = 1 and Q_{n+1} bar = 0 irrespective of the present state.

		यदि E = 1 and D = 1, then S = 1 and R = 0 है . यह latch को set करता है जिस के कारण Q_{n+1} = 1 and Q_{n+1} bar = 0 होता है . अत: यह set state है

The following table shows the **state table** of D flip-flop.

D	Qt + 1t + 1
0	0
1	1

Therefore, D flip-flop always Hold the information, which is available on data input. From the above state table, we can directly write the next state equation as

$$Qt+1= D$$

D flip-flop is always equal to data input, for every positive transition of the clock signal. Hence, D flip-flops can be used in registers, shift registers and some of the counters.

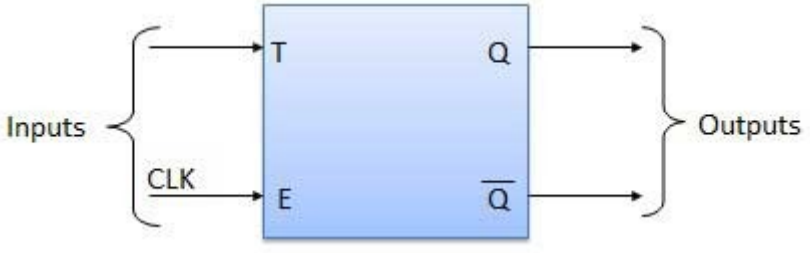
(D flip-flop में डेटा clock signal के every positive transition पर इनपुट के similar होता है। इसलिए, डी फ्लिप-फ्लॉप का उपयोग registers, shift registers and some of the counters में किया जाता है)

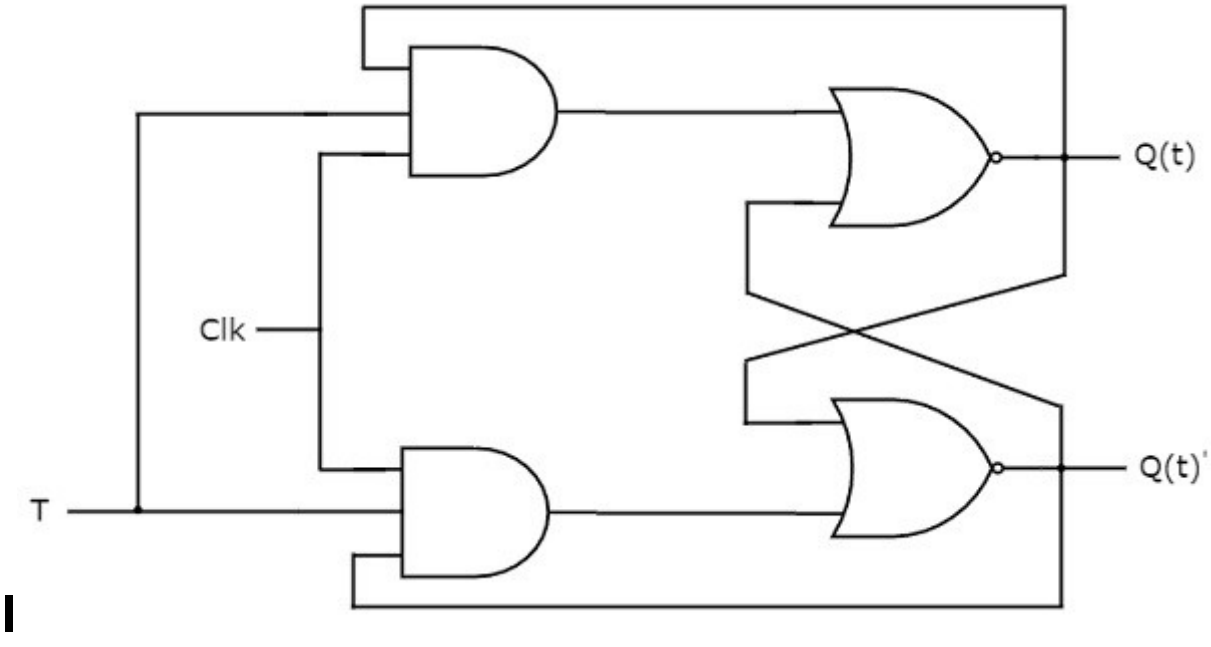
Toggle Flip Flop / T Flip Flop

Toggle flip flop is basically a JK flip flop with J and K terminals permanently connected together. It operates with only positive clock transitions positive clock transitions.

(T FLIP FLOP basically एक JK flip flop है जिसके J and K terminals permanently connected होते है . यह केवल positive clock transitions या positive clock transitions से संचालित होता है।)

Symbol Diagram





Truth Table

Inputs		Outputs		Comments
E	T	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	Q_n	$\overline{Q}_n$	No change
1	1	$\overline{Q}_n$	Q_n	Toggle

Operation

S.N.	Condition	Operation
1	**T = 0, J = K = 0**	The output Q and Q bar won't change
2	**T = 1, J = K = 1**	Output will toggle corresponding to every leading edge of clock

characteristic table of T flip-flop.

Inputs	Present State	Next State
T	**Q**t	**Q**t+1
0	0	0
0	1	1
1	0	1
1	1	0

From the above characteristic table, we can directly write the **next state equation** as

$$Q(t+1)=T'Q(t)+TQ(t)'$$

$$\Rightarrow Q(t+1)=T\oplus Q(t)$$

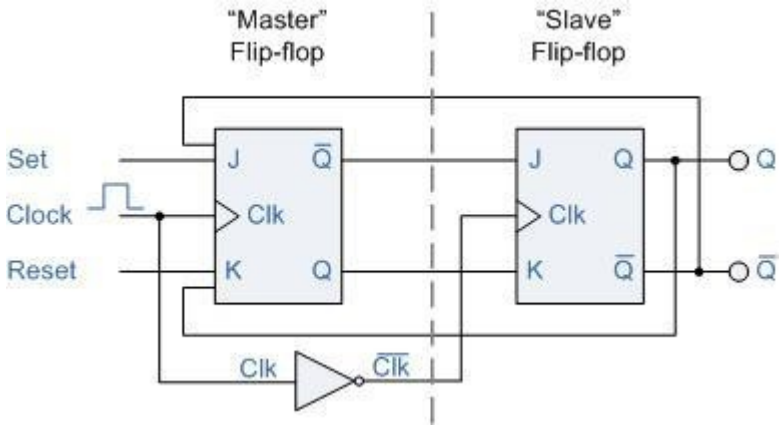
The output of T flip-flop always toggles for every positive transition of the clock signal, when input T remains at logic High 1. Hence, T flip-flop can be used in counters (जब T logic High 1 पर होता है टी T flip-flop का output clock signal के every positive transition पर toggles होता है . अत: T flip-flop का used in counters में किया जाता है).

Master Slave JK Flip Flop

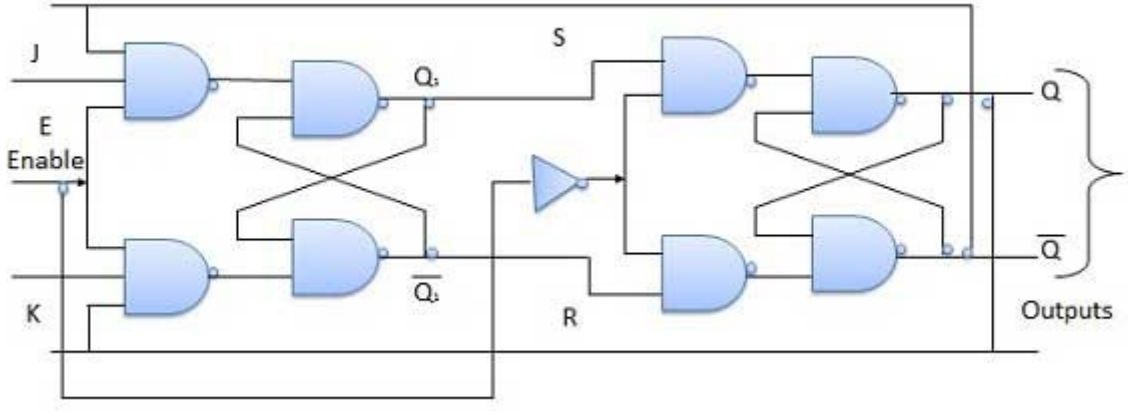
Master slave JK FF is a cascade of two S-R FF with feedback from the output of second to input of first. Master is a positive level triggered. But due to the presence of the inverter in the clock line, the slave will respond to the negative level. Hence when the clock = 1 (positive level) the master is active and the slave is inactive. Whereas when clock = 0 (low level) the slave is active and master is inactive

(Master slave JK FF में two S-R FF का cascade connection होता है जिस में second का output , first के input में feedback होता है. Master positive level triggered होता है तथा slave में negative level triggering होता है. . जब clock = 1 (positive level) होता है to master active होता है and the slave inactive होता है तथा जब clock = 0 (low level) होता है to slave active and master inactive होता है)

Symbol Diagram



Circuit Diagram



Truth Table

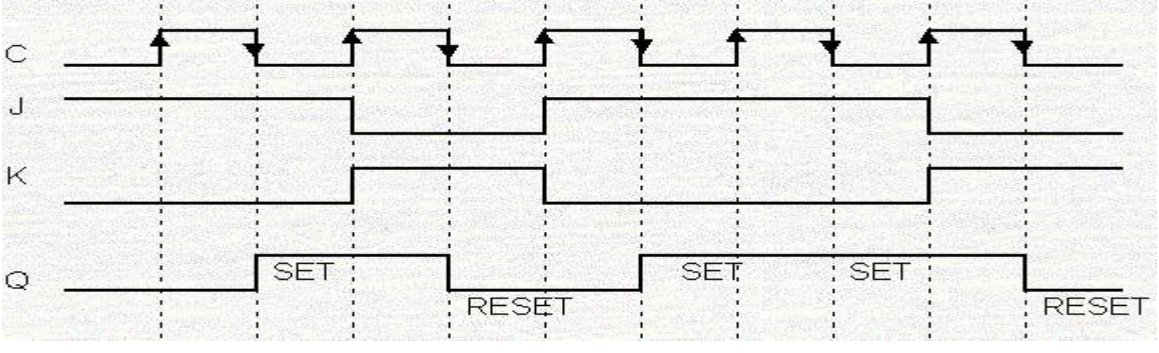
Inputs			Outputs		Comments
E	J	K	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	0	Q_n	$\overline{Q}_n$	No change
1	0	1	0	1	Rset
1	1	0	1	0	Set
1	1	1	$\overline{Q}_n$	Q_n	Toggle

Operation

S.N.	Condition	Operation
1	**J = K = 0 (No change)**	When clock = 0, the slave becomes active and master is inactive. But since the S and R inputs have not changed, the slave outputs will also remain unchanged. Therefore outputs will not change if J = K =0. जब clock = 0 slave सक्रिय हो जाता है और master निष्क्रिय होता है। लेकिन जब S and R inputs नहीं बदले हैं, तो slave का outputs भी unchanged रहेंगा । इसलिए J = K = 0 होने पर आउटपुट नहीं बदलेगा।
2	**J = 0 and K = 1 (Reset)**	Clock = 1 − Master active, slave inactive. Therefore outputs of the master become Q_1 = 0 and Q_1 bar = 1. That means S = 0 and R =1. Clock = 0 − Slave active, master inactive. Therefore outputs of the slave become Q = 0 and Q bar = 1. Again clock = 1 − Master active, slave inactive. Therefore even with the changed outputs Q = 0 and Q bar = 1 fed back to master, its output will be Q1 = 0 and Q1 bar = 1. That means S = 0 and R = 1. Hence with clock = 0 and slave becoming active the outputs of slave will remain Q = 0 and Q bar = 1. Thus we get a stable output from the Master slave.
3	**J = 1 and K = 0 (Set)**	Clock = 1 − Master active, slave inactive. Therefore outputs of the master become Q_1 = 1 and Q_1 bar = 0. That means S = 1 and R =0. Clock = 0 − Slave active, master inactive. Therefore outputs

		of the slave become Q = 1 and Q bar = 0. Again clock = 1 − then it can be shown that the outputs of the slave are stabilized to Q = 1 and Q bar = 0.
4	**J = K = 1 (Toggle)**	Clock = 1 − Master active, slave inactive. Outputs of master will toggle. So S and R also will be inverted. Clock = 0 − Slave active, master inactive. Outputs of slave will toggle. These changed output are returned back to the master inputs. But since clock = 0, the master is still inactive. So it does not respond to these changed outputs. This avoids the multiple toggling which leads to the race around condition. The master slave flip flop will avoid the race around condition.

Master Slave J-K Flip Flop Timing Diagram



- Master slave configuration removes the possibility of race around condition from JK flip flop when we put both J and K as 1 (Master slave onfiguration race around condition की possibility को removes करता है जब both J and K as 1 होता है)
- the output timing is controlled differently in Master slave configuration.(Master slave configuration द्वारा output timing को अलग तरीके से controlled किया जाता है)
- The master stage loads on one edge of the clock waveform and transfers to the slave on the other edge.(master stage में clock waveform के edge लोड होता है और slave पर other edge को loads करता है)